MICROPROCESSOR (8086) BASED PROTECTION SCHEME FOR POWER TRANSFORMERS

by

RAJEEV JAIN

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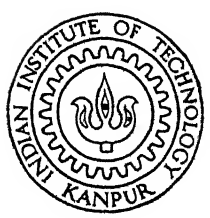

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

JANUARY, 1990

MICROPROCESSOR (8086) BASED PROTECTION SCHEME FOR POWER TRANSFORMERS

A Thesis Submitted

in Partial Fulfilment of the Requirements

for the Degree of

MASTER OF TECHNOLOGY

by

RAJEEV JAIN

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

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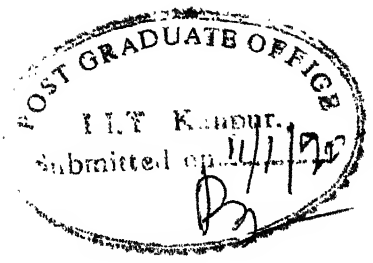
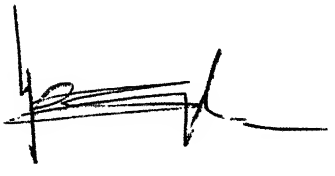


CERTIFICATE

This is to certify that this work entitled MICROPROCESSOR (8086) BASED PROTECTION SCHEME FOR POWER TRANSFORMERS by Rajeev Kumar Jain has been carried out under my supervision and that this work has not been submitted elsewhere for the award of degree.



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ABSTRACT

The responsibility of modern power transformer protection system to provide a comprehensive coverage for more contingencies poses big challenge in the design Of digital relays.This is because of certain problems associated with the transformer like magnetizing and overvoltage inrush currents,tap changing provision ,etc.

In view of the importance of choice of filters, Haar functions have been used to implement FIR filter.

A system has been configured around Intel-8086 microprocessor to realize the digital relay.The possibility of optimum hardware requirement and high speed of operation along with versatility is demonstrated .Tap changing and variable bias factor have also been taken into account. The proposed microprocessor based relaying scheme is efficient,reliable and fast in operation.The scheme has been designed ,fabricated and tested in the lab on a single phase transformer and it is found that it can operate in nearly 10 ms on 50 Hz base.

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CHAPTER 1

INTRODUCTION

The increased complexity, size and power rating of modern power systems has burdened the protective system with the responsibility of providing greater comprehensive coverage for more contingencies than could be justified earlier. Moreover,that the protective systems play decisive role in the reliable operation of complex power system justify that developments in protection techniques should keep pace with the developments in primary systems and the range of products employed for the solution of protection problems to be constantly adopted with regard to functional reliability.Hence,one of the tasks of protection engineer is the conception of relaying scheme to carry out a variety of protective functions reliably and efficiently.

From the implementation point of view,the problem becomes further complicated and challenging due to inherent-and often conflicting - requirements of high reliability and fast operation of protection system.Conflicting because-in the case of digital protection,the domain of present work-high reliability calls for relatively simple hardware,whereas fast opration may require complicated hardware.The advent of VLSI & VVLSI technology,however,has opened exciting new possibilities in the area of protection systems.

Power transformer is an important element of the complex power system.Constant efforts on the part of the manufacturers to reduce their cost,weight and size have resulted in the use of new transformer core materials having higher saturation flux density and a sharp knee point on the B-H curve.also there is an increasing trend to reduce the ratio of saturation flux density to the working flux density from about 1.4 to 1.1.Hence,it is necessary that the protection scheme include protection against overfluxing as well.It is necessary that relay discriminates between inrush and fault conditions.

Though,highly reliable relays for transmission line protection,capable of operating in quarter cycle (5 ms) or less have been designed using travelling wave phenomenon,the same is not true for transformers because it requires unit protection scheme,such as differential relaying.Most of the recent efforts to produce differential relays have been limited either by computational speed requirements (mp 8085) or by limited memory capacity (2920,Analog Signal Processor, Ref.30) or hardware multiplication which leads to poorer reliability.

Now-a-days very fast and powerful microprocessors like 8086,80286,80386 (Intel's) and 68000,68080,68010, 68020,68030 (Motorola's) are available in the market.Using these,multi-relay characteristics can be simulated along with advantages of fast operation and hardware optimization. Exploring the utility of mp8086 in

protection systems has been the chief motivation in inspiring this work.The aim is not to prepare a commercial prototype relaying scheme,because of some basic compromises and laboratory limitations in the work. As will be pointed out later,digital protection schemes offers several advantages over analog ones,and hence,the proposed scheme is a MICROPROCESSOR (8086) BASED,ON-LINE,DIGITAL RELAY FOR TRANSFORMER PROTECTION.

Percentage differential relays for protection of transformers were proposed as early as in 1931,by R.E.Cordray [1].Harmonic restraint to prevent false tripping due to magnetizing inrush current was introduced soon after by Canned by and Hayward in 1938 [2].A relay incorporating these features and a claimed tripping time of around 20 ms (i.e.,nearly one cycle) after the occurrence of the fault was reported by Hayward in 1941 [3].Following this,several other schemes using analog components were added to the literature on the subject [3-4],until G.D.Rockfeller came out with his landmark paper [10] in 1969,discussing the use of digital computer for,*inter alia*,transformer protection.This was followed by another paper in 1972 [11] by Sykes and Morrison,proposing a concrete scheme which could be implemented digitally and giving simulation results to evaluate its performance.This scheme used harmonic restraint to avoid tripping due to the magnetizing inrush current and used infinite impulse response filters to separate harmonics.The resulting scheme was slow in operation and

carried with it all the drawbacks of the analog filters mimicked by it.Later attempts recognized this basic limitation and used digital filtering techniques as they also emerged for various other purposes like digital signal processing,image processing etc.In 1976,Malik,Dash and Hope proposed the use of Fourier Transform Techniques [12] for filtering purposes.Schweitzer,Larson and Flechsig used finite impulse response filters [13] for this purpose.Several other papers by Degens [14],Torp and Phadke [15],Rahman and Dash [16]discussed new ideas like rectangular transformations to minimize multiplications or computational efforts,but still required complex circuitry for implementation.One of the latest papers on the subject explores the use of Haar Transformations to achieve harmonic restraint [17] and proves the feasibility of such scheme.

The study of magnetizing inrush current and efficient algorithms for simulating it are essential for reliable relay design. The first detailed investigation of inrush current and the factors on which it depends was carried out by Blume *et al* [19].Detailed analysis and experiments were carried out to determine the effect of inrush current on relaying [20].Specht suggested some empirical relations to simulate inrush current in a single phase transformer in 1951 [21].Sonnemann *et al* [22] pointed out that the inrush phenomenon in three phase transformers is more complicated than single phase transformers,and some additional considerations are involved.They investigated the suitability

of harmonic restraint for relaying and determined the worst possible waveform against which differential relay has to be tested.Several papers on inrush phenomenon in three phase transformers followed this work including one by Spec ht [23].The most recent approaches reject any functional expression for inrush current,and emphasize that a set of differential eqations has to be solved numerically to simulate inrush current more accurately [24].

References [25] and [26] have used for Infinite Impulse Response filter design while references [27-30] pertain to digital signal processing and Haar function filtering.In the present work the actual hardware design has been carried out using [31-32].

The present work (reported in the thesis) is organized into four chapters,starting with the current one on Introduction.

Chapter 2 reviews critically the existing protection schemes for transformers.Various possible faults are enumerated briefly.Relays to protect the transformer against these faults are described objectively.Some operational problems arising from the implementation point of view have also been discussed.

Chapter 3 is devoted to the proposed digital Proection Scheme of transformer using mp 8086.this chapter is broadly divided into two parts.The first one deals with selection and design of the filters that are to be used for obtaining the fundamental components of differential and mean through

fundamental components of differential and mean through currents,and the second and fifth harmonic components of the differential current.Haar function based FIR filters have been chosen in the present scheme.The second part describes the actual implementation in detail.The hardware design and software developed are also discussed therein.The chapter concludes with performance evaluation of H/W & S/W of the relaying scheme.

Finally,chapter 4 concludes the work with whatever we have been able to achieve and also what we could not.As pointed out earlier the endeavour in this work is not to develop a commercial prototype relaying scheme,but only to demonstrate the feasibility of hardware optimization,with faster speed while retaining the benefits of earlier designs and improving upon them.However,a lot more remains to be done and some suggestions for future work have been given at the end of the chapter.

CHAPTER 2

CRITICAL REVIEW OF EXISTING PROTECTION SCHEMES OF TRANSFORMERS

2.1 INTRODUCTION

Initial part of this chapter deals with a brief description of the faults that are likely to occur in a power transformer. Various protection schemes available for protecting the transformer against these faults have been outlined. The problems associated with the implementation of these schemes like, inrush magnetizing current, over excitation
inrush current, etc. have been pointed out. Finally principle of digital protection schemes being explored now-a-days is discussed briefly.

2.2 FAULTS IN A POWER TRANSFORMER

All cases of abnormal operation (18) in a transformer can be divided into two categories :

1. External Faults
2. Internal Faults.

Former category includes problems like short duration

overloading, short circuits external to the transformer, etc. The primary protection schemes must not operate in such cases.

Internal faults can be divided into the large groups :

(a) INCIPIENT FAULTS :

Though initially these are of a minor nature but slowly they may develop into major fault causing damage to the transformer. Examples of such faults are,

(1) Power electrical connection of conductors or a core fault causing limited arcing inside oil.
(2) Coolant fail re.
(3) Improper oil flow, causing local hot spots developments.
(4) Regul ator faul t s and improper load sharing between parallel transformers causing overheating.

(b) SERIOUS FAULTS :

These can be detected by unbalance of voltage or current at transformer terminals. They can cause immediate damage to the transformer. These are as shown below,

(1) Phase to phase fault on HV,LV (external) terminals
(2) Phase to earth fault on HV,LV (external) terminals.
(3) Phase to phase fault in HV,LV winding.

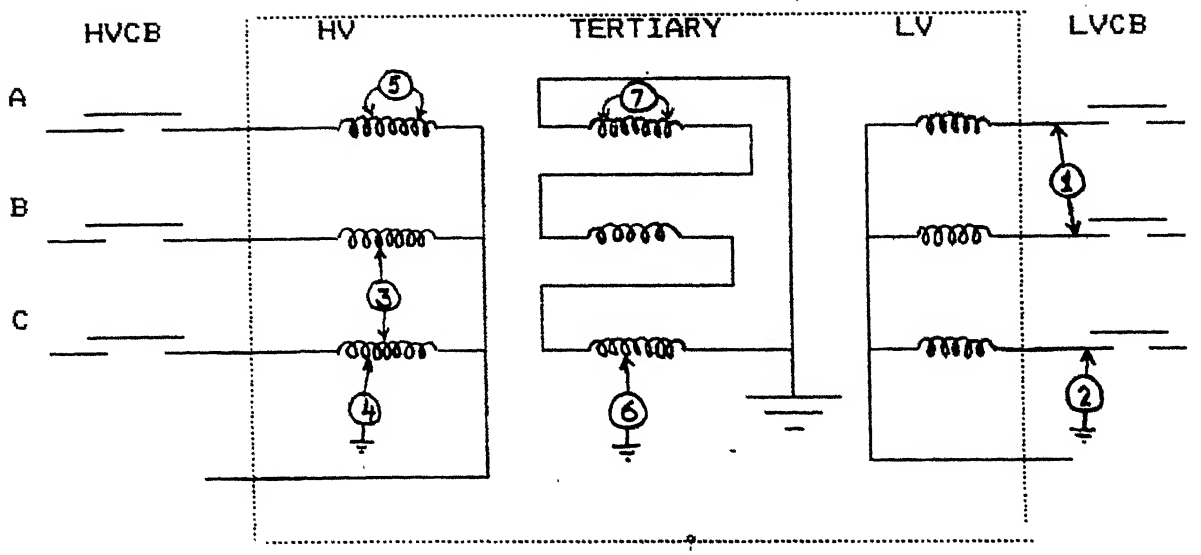

Fig.(2.1) FAULTS IN A TRANSFORMER

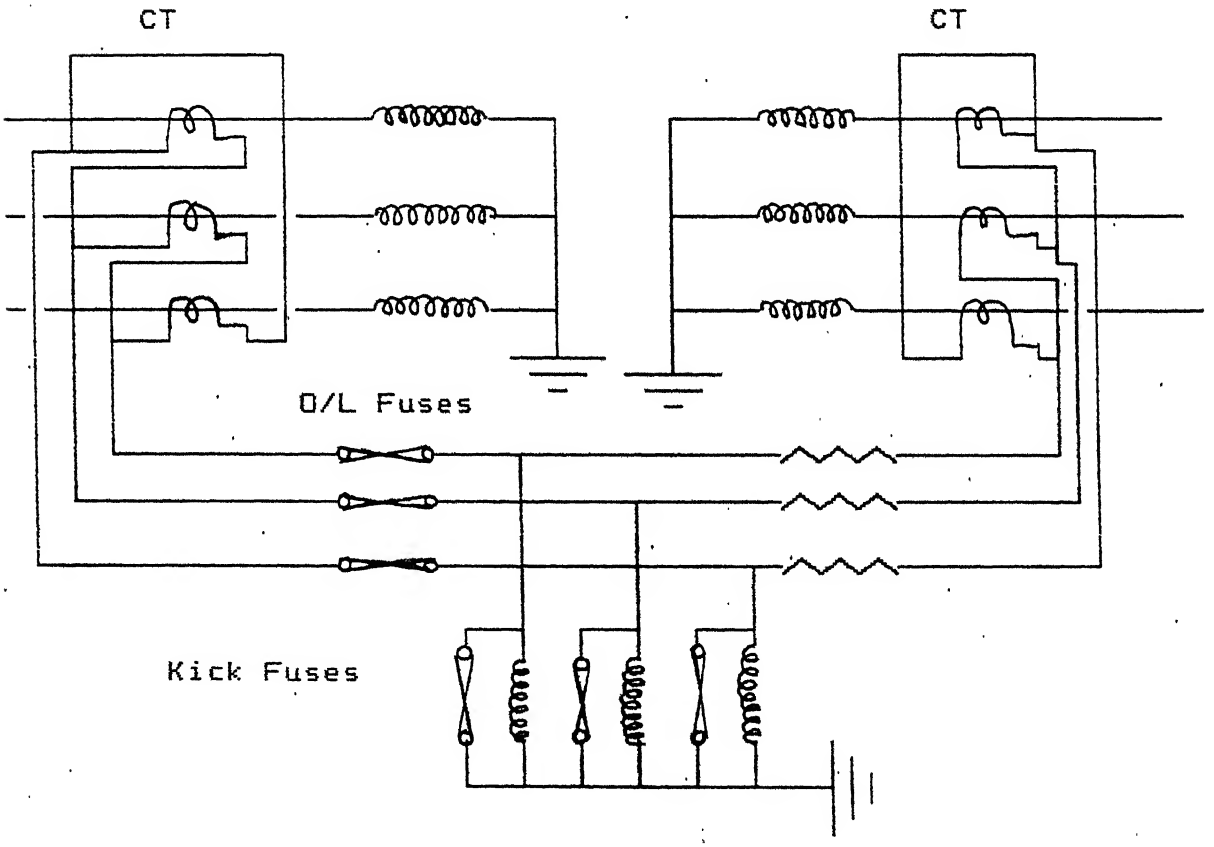

Fig.(2.2) DIFFERENTIAL PROTECTION OF TRANSFORMER

(4) Fault in HV or LV windings (phase to earth).

(5) Short circuit between turns of HV or LV windings.

(6) Earth fault on a tertiary winding

(7) Short circuit between turns of a tertiary winding.

These faults are symbolically represented as shown in the Fig.(2.1).

(9) Sustained system earth fault, and

(10) Sustained system phase to phase fault are examples of external faults.

2.3 PROTECTION SCHEMES USED

For protection of transformer against external faults slow blowing fuses and thermal relays and o.c. relays (back-up protection) have been adopted. The primary transformer protection scheme should not operate in such events. The O/L (overload) fuses shown in the figure 2.2 also provide the back-up protection against through fault, which when sustained can cause damage to the transformer.

Protection against group (a) type of internal faults can be provided by gas relays called Buccholz relay, which has been used widely for several decades now. The relay also responds should the oil level fall due to blockage from the tank. The only limitation is regarding positioning of the relay at the correct angle.

Group (b) faults require fast disconnection. Relays designed for group (b) faults generally will not operate for group (a) faults, and relay designed for group (a) will not be fast enough for group (b) faults. Thus, protection schemes for both the groups are not alternative but supplement to each other.

For group (b) faults, different protection schemes used are as shown below,

(1) Translay protection ,
(2) Magnetic balance protection
(3) Self-stabilizing magnetic balance protection
(4) Differential protection
(5) Biased (percentage) differential protection.

The former three are, however, obsolete now.

The general idea involved in differential protection is to compare operating quantity (voltage or current) at the input and output ends of the equipment being protected. This is a vector comparison, since the quantity being compared has a magnitude and phase angle associated with it. Tripping is initiated if the magnitude of the difference exceeds a pre-determined constant value (or base value).

For a transformer the scheme can be implemented as follows (shown in Fig(2.3)).

Both CTs in above scheme are identical,having the same turn ratio, and I_1' and I_2' represent the currents at two ends of winding. I_1 and I_2 are scaled down version of I_1' and I_2',respectively. The tripping condition is,

$$|\bar{I}_2 - \bar{I}_2| \geq k \qquad \text{;where, k- a constant (base value)}$$

The problem with this scheme is that at large current due to close by external faults even though I_1' and I_2' are equal, I_1 and I_2 may be significantly different due to CT errors caused by different level of saturation of CTS.To avoid this,a relaying scheme called percentage (biased) differential protection or BDP is devised in which the magnitude of $(\bar{I}_1-\bar{I}_2)$ operating quantity and the mean through current $(\bar{I}_1+\bar{I}_2)/2$ restraining quantity are compared.The tripping criterion now becomes,

$$|I_1-I_2| \geq S\,|I_1+I_2/2| \qquad S - \text{bias factor}$$

Practically,the two CTs have to be of different turn ratios because I_1' and I_2' are not equal for normal operation If N_1/N_2 is the turn ratio of the power transformer being protected then $I_1/I_2=N_2/N_1$ ignoring magnetizing current which is small as compared to load currents.

Hence, turn ratios of the CTs are in the same proportion as the turn ratio of the power transformer being protected.

Further, to take care of the phase shift due to different winding connections on the two sides of the main transformer, the CTs are connected with opposite connections as shown in Fig.(2.).

2.3.1 THE RELAY CHARACTERISTICS :

Threshold characteristics of aPBD relay are now examined.

Let current I_1 is the reference, i.e., $\bar{I}_1 = \bar{I}_1 \angle \theta$ and $\bar{I}_2 = \angle \phi$, then

$$\bar{I}_1 + \bar{I}_2 = I_1 \angle \theta^{\circ} + I_2 \angle \phi$$

$$= I_1 + I_2 (\cos\phi + j \sin\phi) \qquad \ldots 2.1$$

and $$\bar{I}_1 - \bar{I}_2 = I_1 - I_2 (\cos\phi - j \sin\phi) \qquad \ldots 2.2$$

The threshold condition is

$$|\bar{I}_1 - \bar{I}_2| = \frac{1}{2} S |\bar{I}_1 + \bar{I}_2| \qquad \ldots 2.3$$

Squaring both sides, we get

$$|\bar{I}_1 - \bar{I}_2|^2 = \frac{1}{4} S^2 |\bar{I}_1 + \bar{I}_2|^2 \qquad \ldots 2.4$$

Substituting from earlier expressions :

$$(I_1 - I_2 \cos\phi)^2 + (I_2 \sin\phi)^2 = \frac{S^2}{4} [(I_1 + I_2 \cos\phi)^2 + (I_2 \sin\phi)^2] \qquad \ldots 2.5$$

Dividing by I_1^2 and simplifying :

$$(1 - \frac{S^2}{4}) (\frac{I_2}{I_1}) + 2 (1 + \frac{S^2}{4}) (\frac{I_2}{I_1}) \cos\phi = \frac{S^2}{4} - 1 \qquad \ldots 2.6$$

Dividing by $(1 - \frac{S^2}{4})$ and then adding $(\frac{4+S^2}{2})$ to both the sides,

$$\frac{I_2^2}{I_1^2} + 2\left(\frac{I_2}{I_1}\right)\left(\frac{4+S^2}{4-S^2}\right)\cos\phi + \left(\frac{4+S^2}{4-S^2}\right) = \left(\frac{4+S^2}{4-S^2}\right) - 1 = \frac{10S}{(4-S^2)^2} \quad \ldots 2.7$$

Now, let,

$C = \frac{4+S^2}{4-S^2}$, $\gamma = \frac{4S}{4-S^2}$ and $\beta = \frac{I_2}{I_1}$ then, substituting in above

$$\boxed{\beta^2 - 2\beta C\cos\phi + C^2 = \gamma^2} \quad \ldots 2.8$$

This is equation of a circle in polar co-ordinates.

2.3.2 REASONS FOR TAKING HIGH BIAS FACTOR FOR TRANSFORMERS

The bias factors for transformers varies from 0.1 to 0.5 while that for generators it is in the neighborhood of 0.05 .Following are the reasons for this:

(1)- MAGNETIZING STEADY STATE VALUE CURRENT

A permanent mismatch is created between primary and secondary sides due to this component of current (nearly 5% of F.L.current).

(2)- C.T.CHARACTERISTICS:

Due to standardization of CTs available in the market,finding one with exact turn ratio is not possible.This leads to difference in the currents supplied to relay even under normal conditions.

Moreover,due to different turn ratio of CTs used, the cores may not saturate to the same extent in the event of high mean through currents resulting from a close-by external fault .This may lead to error in the current being monitored.

(3)- TAP CHANGING

CTs are not provided with tap changing provision which is available on power transformers and hence the unbalanced current may flow through differential relay as the transformer turn ratio is changed from nominal value,using tapping,to improve the voltage profile.

The following phenomena lead to false operation of the relay:

MAGNETIZING INRUSH CURRENT :

This current flows in primary windings when the transformer is switched on with secondary windings open circuited. The magnitude of this current may be 10 to 15 times the rated current and may last for nearly 2 seconds as this current decays very slowly due to large magnetizing

inductance.

The phenomenon is much more complex in 3-ϕ transformers, because the current flowing in one winding is dependent on the currents in other windings as well.

Factors affecting the magnitude of the magnetizing inrush current are as follows :

(1) quality of steel used for core construction,

(2) the level of residual magnetism,

(3) its polarity,

(4) the instant of switching-in [19-24].

For relaying purpose, it is sufficient to know that the second harmonic contents of inrush current waveform is never expected to be less than 16% [22]of the fundamental;fo r both 1-ϕ and 3-ϕ transformers. This phenomenon has been used to discriminate current imbalances due to internal faults and due to inrush currents.

The 'Kick fuse' shown in Fig.(2.4) is also used in circuit only during the period of switching-in.

OVERVOLTAGE INRUSH CURRENT :

Over voltages as high as 20 to 50% result from sudden loss of load. Since modern transformers operate near saturation flux levels, such over voltages cause a very large increase in excitation current which may be as large as 10 to 100 times. It may sustain for long and may cause false operation of a differential relay.

Third harmonic contents in this case increase considerably. Though, this can be used for overvoltage inrush recognition, it is not always available because of delta connections. Thus, relaying operation can be by using only fifth harmonic, which is also present in overvoltage inrush excitation current to a significant extent. Third harmonic monitoring needs additional hardware.

The imbalance between primary & secondary due to above factors is annulled by taking higher value of 'S'. False operation of relay due to magnetization and overvoltage inrush currents can be prevented by monitoring the second and fifth harmonics of the differential current respectively.

2.4 OVERVIEW OF PROTECTION SCHEMES :

Initial differential relays were electromechanical. These suffered from following disadvantages :

(1) higher burden on instrument transformers (CTs and PTs)

(2) slow operation

(3) contact racing and pitting

(4) high maintenance requirements

(5) false operation due to shocks or vibrations caused by external factors such as movement of Diesel or electric locomotives, tram cars or earthquakes etc.

With the development of electronic valves, some electromechanical relays were replaced by electronic ones. This is because of the following reasons :

(1) imposed low burden on instrument transformers

(2) had no contacts or moving parts

(3) were easy to maintain

(4) were very fast in operation

(5) have none of the drawbacks of electromechnical relays.

In spite of this, they did not find very easy acceptance, because of drawbacks like high quiescent power consumption, very high battery voltage requirement, voluminous circuitry, and uncertain life of valves.

As a result, valves were replaced by transistors as soon as they became available. These static relays proved to be :

(1) stable

(2) reliable

(3) compact in size

(4) cheaper

(5) faster in operation

(6) shock-proof

(7) requiring very little power & maintenance (repair)

(8) more sensitive

(9) permitting the use of smaller and simple CTs

(10) realizing more sophisticated characteristics.

The only major drawbacks of static relays are,

(1) complexity

(2) change in threshold characteristics with time and use (aging effect).

Both these problems have been overcome with the

introduction of digital relays. There has been increasingly tendency to use these relays ever since the advent of microprocessors. Initial schemes proposed the use of off-line central digital computer for protection. More recent efforts focus on inexpensive, reliable, very fast microprocessor based relays. The main advantages of these relays are:

(1) possibility to realize different types of sophisticated threshold characteristics of relays with the same piece of hardware or with the minimum changes in hardware.

(2) Easy to change the setting of the relay for alternation in system conditions.

(3) Ability to check correctness of input & data missing or incorrect information (self correcting).

(4) Possibility of interfacing with other devices.

(5) Less maintenance is required.

(6) It reduces relay types, spare parts & documentation.

(7) It can give fault reports without specially designed devices for post fault analysis.

(8) Impose very low burden on CTs unlike electromagnetic types.

(9) While the cost of conventional relay is steadily rising, those of digital processors suitable for apparatus of protection are slowly decreasing.

(10) Self checking type.

2.4.1 REVIEW OF VARIOUS RELAYING ALGORITHMS :

These are algorithms using flux restraint or differential equation models of transformer. In most of the cases, it is essential to measure currents in all transformer windings to use algorithms. They also use either B-H curve data or equivalent circuit parameters.

The flux restraint scheme, suggested by Phadke & Thorp [31], uses flux current relationship of the transformer to obtain the restraint function. It was claimed that it leads to a secure transformer protection algorithm. As the flux level is direct measure of saturation, it is the most basic variable to be used to generate restraint function.

As far as the filtering is concerned, techniques like Ha ar function, Walsh function & Kalman filtering has been used. The digital protection scheme using Walsh transformation [33] uses even & odd rectangular waves for extracting the fundamental and second harmonic component phasor from sampled values of primary & secondary currents of transformer. This, however, does not provide protection against overvoltage inrush current. The Kalman filtering technique [34] for designing protection algorithm used state space models of sinusoidal and decaying d.c. signals. The results shown in the paper were satisfactory. However, it is not known whether the technique has been used to design the protection scheme. The present work uses Haar filtering to be described later.

New techniques describes a 1-ϕ transformer relay that uses time based logic to discriminate between magnetizing

inrush & internal faults. Three such relays are needed for differential protection of 3-phase transformer.

Recently a new algorithm is proposed by Sachdev et al. [32], it does not use the presence of harmonic currents or B-H curve or equivalent circuit parameters, to restrain the relay during magnetizing inrush unlike previous algorithms. It is suitable for situations it either is or net possible to measure the winding currents. It exploits the fact that the electromagnetic equations of a transformer are differential equation of voltages, currents and mutual flux linkages. The equations are valid during magnetizing inrush, normal operating conditions and external faults. However, they are not valid during internal faults. As the mutual flux linkages of the primary and secondary winding of a single phase (and each phase of a three phase transformer) represent equal voltage/turn, the approach also takes into consideration the non-linearity of the transformer core without explicitly using this characteristic in algorithm. This makes algorithm less complicated & computationally more efficient.

It is claimed that the algorithm successfully blocks tripping during magnetizing inrush & external faults and issues trip commands on occurance of internal faults. It, however, also does not take care of overvoltage inrush current. It is as sensitive to low level faults as to high level ones. Computational requirements are modest.

CHAPTER 3

PROPOSED DIGITAL PROTECTION SCHEME OF TRANSFORMER

3.1 INTRODUCTION

The present chapter discusses the proposed relaying scheme for the protection of transformer. It is a novel relaying scheme using microprocessor 8086 and digitalfilter based upon Haar Transform has been used to monitor fundamental, 2nd and 5th harmonics component of the current.The microprocessor based relaying scheme has been designed, fabricated and tested in the lab.

3.2 PRELIMINARY

While writing the tripping criterion to PBD relay, viz.,

$$|\bar{I}_1 - \bar{I}_2| \geq S\left|\frac{\bar{I}_1 + \bar{I}_2}{2}\right|$$

it is explicit that I_1 and I_2 are pure sinusoidal waveforms. This, however, is not true in practice where the current waveform consists of both, the fundamental as well as several harmonic components and hence the resulting wave can be usedonly if fundamental components of differential and mean through currents are obtained by appropriate filtering scheme. The condition for tripping, now becomes,

$$|\bar{I}_1 - \bar{I}_2|_1 \geq S\left|\frac{\bar{I}_1 + \bar{I}_2}{2}\right|_1 \qquad 3.1$$

Also, to make the relay immune so as to avoid tripping due to magnetizing and overvoltage inrush currents, second and fifth harmonic components which are contained in these currents, are also needed. On the basis of results obtained by Rockfeller et al. (22), the inrush condition exists when,

$$|I_1 - I_2|_2 \geq 0.16\ |\bar{I}_1 - \bar{I}_2|_1 \qquad 3.2$$

AND/OR

$$|I_1 - I_2|_5 \geq K\ |\bar{I}_1 - \bar{I}_2|_1 \qquad 3.3$$

Combining the above three conditions (Eqns. 3.1 - 3.3), the final tripping criterion will be as shown below,

$$\left.\begin{array}{l} |\bar{I}_1 - \bar{I}_2|_1 \geq S\left|\dfrac{\bar{I}_1 + \bar{I}_2}{2}\right| \\ \text{AND} \quad |\bar{I}_1 - \bar{I}_2|_2 \geq 0.16\ |\bar{I}_1 - \bar{I}_2|_1 \\ \text{AND/OR} \quad |I_2|_5 \geq K\ |\bar{I}_1 - \bar{I}_2|_1 \end{array}\right\} \qquad 3.4$$

where K is a scalar.

This tripping criterion makes the relay inrush proof. This task can be algorithamised in the following ways.

(i) Obtain samples of I_1 and I_2, convert them to the digital form and determine (I_1-I_2) and $(\frac{I_1+I_2}{2})$.

(ii) Extract RMS valves of (I_1-I_2), $(I_1-I_2)_2$, $(I_1-I_2)_5$ and $(\frac{I_1-I_2}{2})$.

(iii) Trip after testing tripping criterion of Eqn.3.4.

The relaying scheme is represented by the block diagram shown in Fig.(3.1).

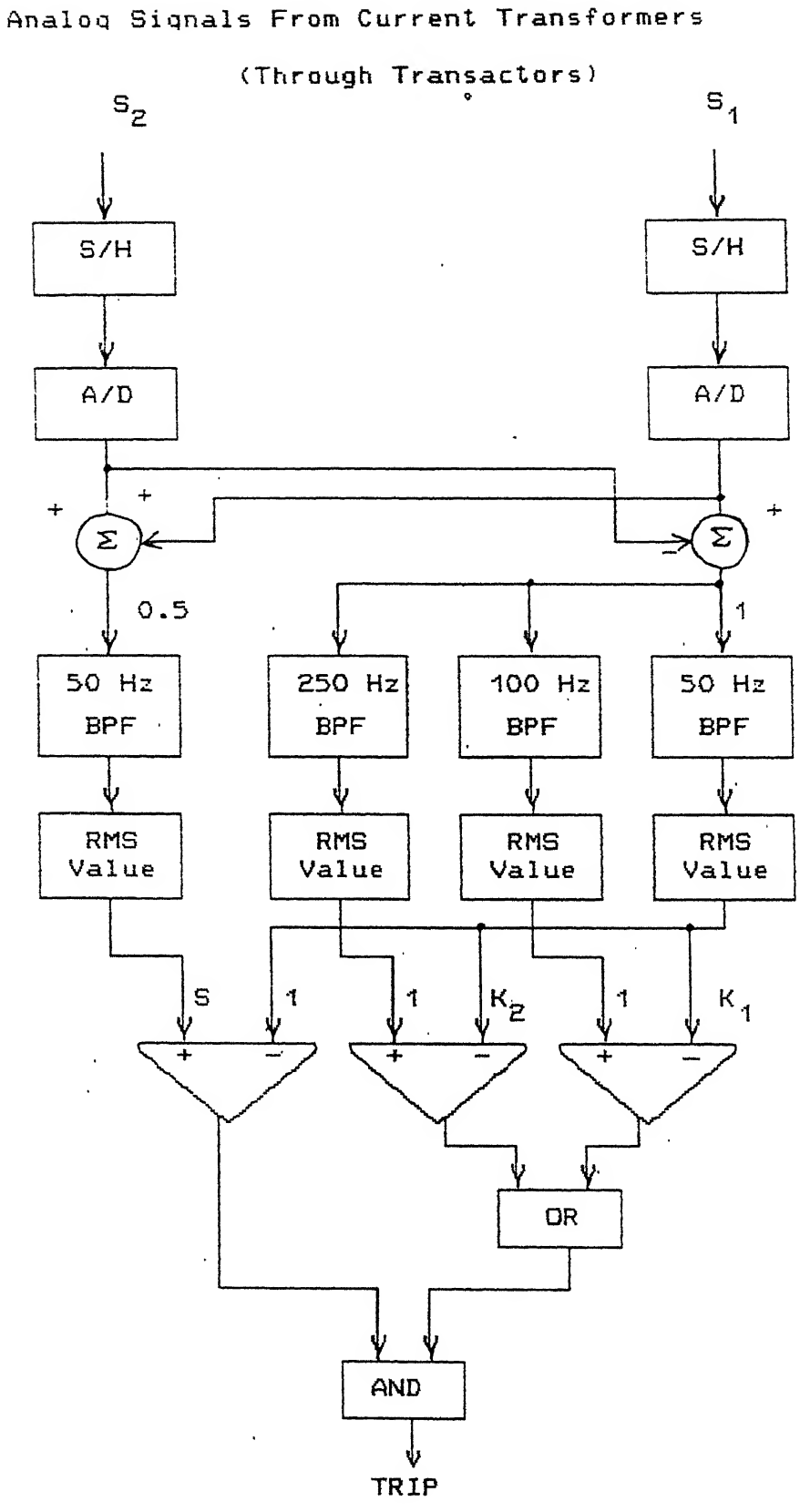

Fig.(3.1) BLOCK DIAGRAM OF PERCENTAGE DIFFERENTIAL RELAY

3.3 FILTER SPECIFICATIONS

It is evident, that, in the present relaying scheme three filters viz. 50 Hz, 100 Hz, 250 Hz Band Pass need to be designed.

The 250 Hz filter must reject 50 Hz and 100 Hz frequencies adequately .If 30 dB is the attenuation of 50 Hz and 100 Hz, by 250 Hz filter, the 'leakthrough' will be around 3%, that appears reasonably small. We assume that we require around 30 dB attenuation for 50 Hz and 100 Hz. Similarly, 100 Hz BPF can also be designed for 30 dB attenuation for 50 Hz, 100 and 250 Hz components.

Hence 250 & 100 Hz filters can be specified as the ones which have the center frequencies of 250 Hz and 100 Hz & provide nearly 30 dB attenuation at 50 Hz, 100 Hz & 250 Hz and at other frequencies. The frequency response is not of any great importance to us, but all harmonics and offset must be attenuated sufficiently.

The constraints on 50 Hz filter will be much less stringent, because the 50 Hz component dominates all other components of the signal in the power system. Hence 250 and 100 Hz filters are bottleneck in improving response time. The filtering technique and their choice is discussed in the following para.

3.3.1 CHOICE OF FILTERING TECHNIQUE :

Two types of digital filters are in practice viz.

Filter Type	Order	3 dB BW	5% settling time
Butterworth	2	15.0	97.2
	3	25.0	74.2
	4	32.0	93.2
	5	37.5	89.8
	6	42.2	88.9
	7	45.0	107.6
Chebyshev,0.01 dB ripple	2	15.0	56.7
	3	25.0	72.2
	4	37.5	74.1
	5	44.1	72.5
	6	50.0	71.5
	7	55.0	85.0
	8	59.0	85.9
Legender	2	14.4	62.1
	3	27.3	62.0
	4	37.7	56.2
	5	45.7	72.0
	6	51.9	69.9
	7	56.9	80.4

TABLE 2.1 COMPARISION OF VARIOUS ANALOG FILTERS

non-recursive filters, where the output is a function of only the previous & present inputs. They are also called Finite Impulse Response filter. The other, recursive filter (Infinite Impulse Response) filter are the ones where, by using feedback, the output becomes a function of past & present inputs & outputs.

Though the traditional approach has been to use IIR filters whose design involves transforming an analog filter into a digital filter that meets the prescribed specifications, they offer disadvantages like non-linearity in phase .

On the other hand, FIR filter offer several advantages. They can be designed to have exactly linear phase, thus preventing any phase distortion of the input signal. Due to their non-recursive nature, FIR filters are always stable. However, a strong disadvantage is that a large number of delay elements are needed to obtain a sharp cutoff, thereby requiring a large amount of processing.

Another option left open is to use any one of the transform domains employed in image processing. A brief comparison of these transforms is given in table (3.1), which is reported partly from (27).

A fourier transform would give the harmonic amplitudes directly. If we use any other transform & wish to obtain the harmonic contents some subsequent processing will be required. The table (3.2) indicates that Haar transform achieves a drastic reduction in the required computational efforts. This is born out by previous attempts using F T (12) & Haar transform (17).

In view of the facts mentioned above, it will be desirable to use Haar transform for filtering. A brief review of Haar functions & their use in digital filtering follows.

3.3.2 HAAR TRANSFORM BASED FILTERS :

The Haar functions form a complete set of orthogonal rectangular functions. Introduced by Hungarian mathematician Alfred Haar, it describes a set of orthogonal functions, each taking essentially two values & yet providing an expansion of a given continuous function, which could be made to converge rapidly & uniformly. These functions provide some computational advantages in certain areas of communication, image coding and digital filtering.

For a time interval $0 \le t \le T$, the Haar function is defined as,

$$HAR(2^p+n,t)=\begin{cases} \sqrt{2^p} & \text{for } \frac{n}{2^p} \le t \le (n+\frac{1}{2})/2^p \\ -\sqrt{2^p} & \text{for } (n+\frac{1}{2})/2^p \le t \le (n+1)/2^p \\ 0 & \text{otherwise.} \end{cases}$$

The first 16 Haar functions are shown in Fig.(3.2).

It can be shown from the definition that

$$\int_0^1 HAR(m,t)HAR(n,t)dt = \begin{cases} 1 & \text{for } n=m \\ 0 & \text{for } n\neq m \end{cases}$$

This constitutes the property of orthogonality.The proof of completeness is given by Haar(28).Thus,Haar functions as described above form a complete set of orthogonal functions.

Any given continuous periodic function,with a time

period T=1, can be synthesized from a Haar series by

$$f(t) = \sum_{n=0}^{\infty} C_n \, HAR(n,t) \qquad 3.5$$

where, $$C_n = \int_0^1 f(t).HAR(n,t)dt \qquad 3.6$$

The convergence features of Haar series have been shown by Alexits (29). It has been shown by Shore (30) that, a comparatively smaller number of terms are necessary to approximate a waveform using the Haar series.

If a function is f(t) is specified by N samples (X_1, X_2 $X_3 \ldots X_n$) during a time period, a Haar series can not be used for it. However, a discrete Haar transform and its inverse can be defined from Eqns.(3.5 and 3.6) as,

$$X_n = \frac{1}{N} \sum_{i=0}^{N-1} C_i \, HAR\,(n,i/N)$$

$$C_i = \sum_{n=0}^{N-1} X_n \, HAR\,(n,i/N)$$

$i,n = 0,1,2,3,\ldots,N-1$

Written in the matrix form, these equations become,

$$[X]_{N\times 1} = \frac{1}{N} [H]_{N\times N} [C]_{N\times 1} \qquad \ldots 3.7$$

and

$$[C]_{N\times 1} = [H]^{-1}_{N\times N} [X]_{N\times 1} \qquad \ldots 3.8$$

where, $[H]$ is the Haar function matrix and $[H]^{-1}$ is its inverse. $[H]^{-1}$ is simply given by the transpose of $[H]$, because

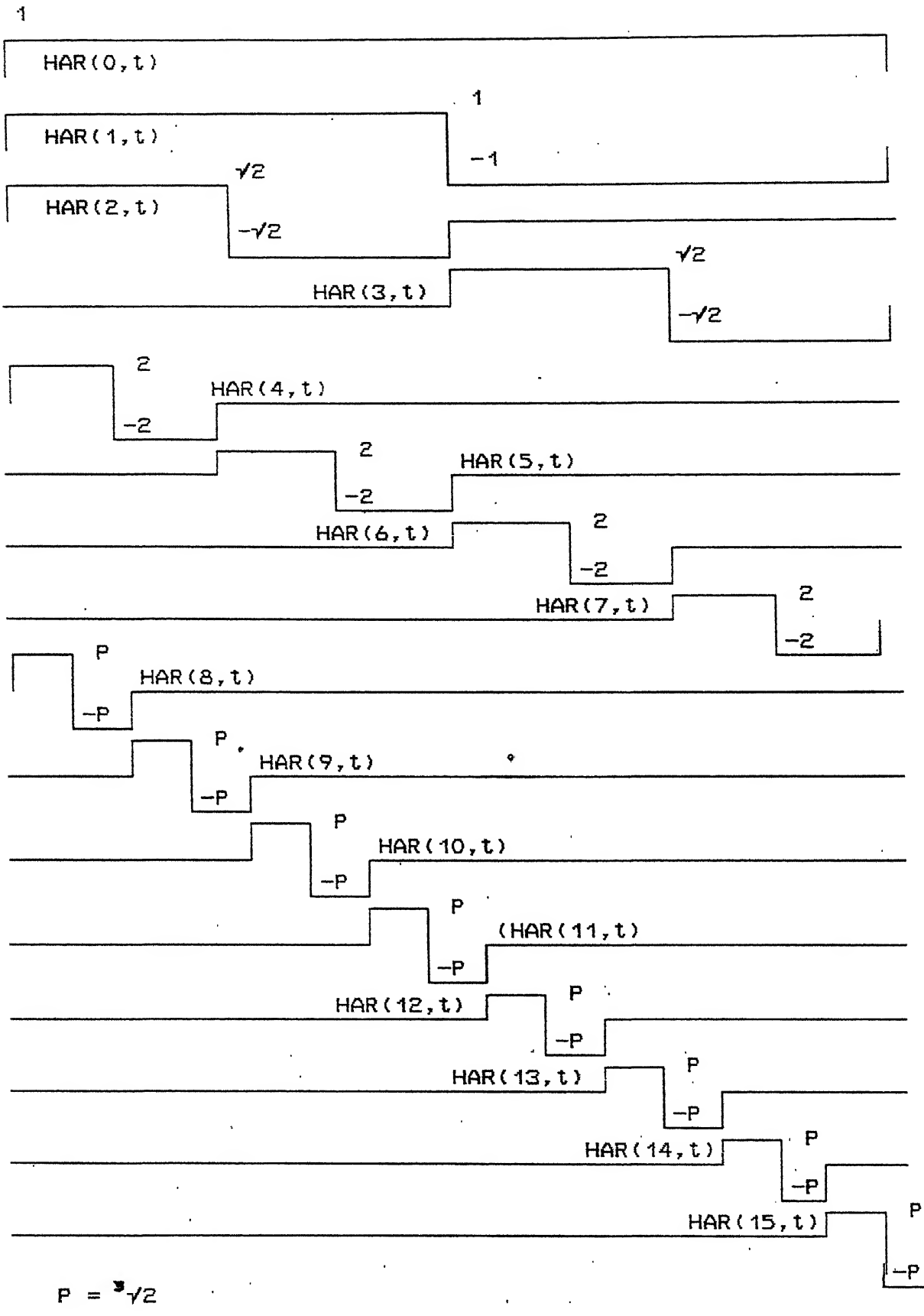

Fig.(3.2) FIRST 16 HAAR FUNCTIONS

of the orthogonality property. For N=16,the matrix [H] will be

$$H = \begin{bmatrix}
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\
\sqrt{2} & \sqrt{2} & \sqrt{2} & \sqrt{2} & \sqrt{2} & \sqrt{2} & \sqrt{2} & \sqrt{2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} \\
2 & 2 & -2 & -2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 2 & 2 & 2 & 2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 2 & 2 & -2 & -2 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 2 & 2 & -2 & -2 \\
2\sqrt{2} & 2\sqrt{2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 2\sqrt{2} & 2\sqrt{2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 2\sqrt{2} & 2\sqrt{2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 2\sqrt{2} & 2\sqrt{2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -2\sqrt{2} & -2\sqrt{2} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -2\sqrt{2} & -2\sqrt{2} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -2\sqrt{2} & -2\sqrt{2} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -2\sqrt{2} & -2\sqrt{2}
\end{bmatrix}$$

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If this transformation is carried out directly, N^2 operations are required. However, if a factorisation algorithm similar to the one used for fast Fourier Transform is used, the total number of operations can be reduced to $2(N-1)$. A diagram for the 16 point fast Haar Transform is shown in Fig.(3.3). The solid lines are addition and the broken lines are subtraction at the nodal points. The multiplications

have all been delayed until the transformation is complete.The Haar coefficients are as follows :

$$C_0^{\cdot}=C_0= X_0+X_1+X_2+X_3+X_4+X_5+X_6+X_7+X_8+X_9+X_{10}+X_{11}+X_{12}+X_{13}+X_{14}+X_{15}$$

$$C_1^{\cdot}=C_1= X_0+ X_1+X_2+X_3+X_4+X_5+X_6+X_7-X_8-X_9-X_{10}-X_{11}-X_{12}-X_{13}-X_{14}-X_{15}$$

$$C_2=\frac{C_2}{2}=X_0+X_1+X_2+X_3-X_4-X_5-X_6-X_7$$

$$C_3^{\cdot}=\frac{C_3}{2} = X_8+X_9 +X_{10}+X_{11}-X_{12}-X_{13}-X_{14}-X_{15}$$

$$C_4^{\cdot}= \frac{C_4}{2}= X_0+X_1-X_2-X_3$$

$$C_5^{\cdot}= \frac{C_5}{2}= X_4+X_5-X_6-X_7$$

$$C_6^{\cdot}= C_6/2= X_8+X_9-X_{10}-X_{11}$$

$$C_7^{\cdot}= C_7/2= X_{12}+X_{13}-X_{14}-X_{15}$$

$$C_8^{\cdot}= C_8/2\sqrt{2} = X_0- X_1$$

$$C_9^{\cdot}= C_9/2\sqrt{2} = X_2-X_3$$

$$C_{10}^{\cdot}= C_{10}/2\sqrt{2} = X_4-X_5$$

$$C_{11}^{\cdot}= C_{11}/2\sqrt{2} = X_6-X_7$$

$$C_{12}^{\cdot}= C_{12}/2\sqrt{2} = X_8-X_9$$

$$C_{13}^{\cdot}= C_{13}/2\sqrt{2} = X_{10}-X_{11}$$

$$C_{14}^{\cdot}= C_{14}/2\sqrt{2} = X_{12}-X_{13}$$

$$C_{15}^{\cdot}= C15/2\sqrt{2} = X_{14}-X_{15}$$

the above scheme , the Fourier series coefficients can be obtained as derived below :

Let,

$$f(t)= F_0 + \sqrt{2}F_1 \sin \frac{2\pi}{T} t + \sqrt{2}F_1 \cos \frac{2\pi}{T} + \sqrt{2}F_3 \sin \frac{2\pi}{T}$$

$$+ \sqrt{2}F_4 \cos \frac{2\pi}{T} t + \ldots \qquad \ldots 3.9$$

It can be assumed , without loss of generality, that the fundamental time period T=1. The coefficients $F_1, F_2, \ldots$ are given by

$$F_1= \sqrt{2} \int_0^1 f(t) \sin 2\pi t \, dt$$

$$F_2= \sqrt{2} \int_0^1 f(t) \cos 2\pi t \, dt$$

$$\vdots$$

Now, $f(t)= \sum_{n=0}^{\infty} C_n HAR(n,t)$. It follows from equation above that

$$F_1= \sqrt{2} \int_0^1 \left[\sum_{n=0}^{\infty} C_n HAR(n,t) \right] \sin 2\pi t \, dt$$

$$= 0.9C_1+0.1865(-C_4+C_5+C_6+C_7) + \ldots$$

We are using discrete Haar transform with N=16,hence

$$F_1=0.9C_1+0.1864(-C_4-C_7)+0.1816(C_5+C_6)$$

$$+.0896(-C_8+C_{11}+C_{12}-C_{15})+ 0.03705(-C_9+C_{10}+C_{13}-C_{14}) \qquad \ldots 3.10$$

$$F_2=0.6366(C_2-C_3)+ 0.1864(C_4+C_5-C_6-C_7)$$

$$+0.03705(C_8+C_{11}-C_{12}-C15)+ 0.0896(C_9+C_{10}-C_{13}-C_{14})$$

...3.11

$$F_3=0.6366(C_2+C_3)+... \qquad ...3.12$$

$$F_4= 0.6366(C_4-C_5+C_6-C_7)+... \qquad ...3.13$$

$$F_5= 0.18C_1+0.1273(C_4-C_5-C_6+C_7)+0.1347(C_8-C_{11}-C_{12}+C_{15}) +0.3252(C_9+C_{10}+C_{13}-C_{14}) \qquad ...3.14$$

$$F_6= 0.1273(-C_2+C_3)+0.1536(C_4+C_5-C_6-C_7) +0.3252(-C_8-C_{11}+C_{12}-C_{15})+ 0.1347(C_9+C_{10}-C_{13}-C_{14}) \qquad ...3.15$$

The modified Haar coefficient ($C_0^*, C_1^*...$) are to be used to write the final relations for F_i^*s.

The RMS values of the first second and fifth harmonic are given by

$$A_1 = \sqrt{F_1^2+F_2^2} \qquad ...3.16$$

$$A_2 = \sqrt{F_3^2+F_3^2} \qquad ...3.17$$

$$A_5 = \sqrt{F_4^2+F_5^2} \qquad ...3.18$$

The frequency response of the filter so obtained is found to be satisfactory [37]. The response is such that all undesirable frequencies are rejected adequately, if the operating frequency is 50 Hz.Performance degrades severely

with change in frequency.

The feasibility and attractiveness of Haar Transform based filters is exploited here in designing the digital relay.

3.4 PROPOSED RELAYING SCHEME

This part describes the actual integrated solution that has been implemented to overcome most of the difficulties envisaged and presents the results of some studies carried out to determine the performance of the relay .The scheme developed at present is for single phase transformer which could be extended to 3-ϕ transformers with modifications.The scheme has been implemented on intel's 8086 processor.

3.4.1 BASIC SCHEME

Current imbalance between primary and secondary CTs may occur either because of an internal fault or due to inrush current caused by overvoltage.The relay has to sense the actual situation using the samples and accordingly has to take the decision of tripping or no-tripping.To meet the time constraints,for the processing time, the 16-bit Intel's 8086 microprocessor has been used.

3.4.2.1 TAP CHANGING

To account for the mismatch created by tap changing in a power transformer,one of the sampled current is multiplied by a correction factor.For this purpose an analog input,indicating a tap setting, is provided to the relay.The value of this third input can be varied between +1.0 and -1.0,and the correction factor used is $(1+\frac{TAP}{8})$ in other

words,samples of I_1 are replaced by $I_1(1+TAP/8)$.With this provision ,tap setting changes up to ± 12.5% from the nominal value can be incorporated.

3.4.2 VARIABLE BIAS FACTOR

The problems of current transformer mismatch etc. are less severe when the currents I_1 and I_2 are small .this means that we can use a smaller value of bias factor 'S'when the mean through current $\left(\frac{I_1+I_2}{2}\right)$ is small,leading to more sensitive relaying.However ,'S' has to be increased as the mean through current becomes larger and CTs begin to saturate.

The bias factor used here is directly proportional to the mean through current and is given by

$$S= \left(\frac{I_1+I_2}{2}\right)_{rms}+0.0625$$

It can be noted that,for the relay developed,S can vary between 0.065 & nearly 0.77 under the worst possible condition For normal load currents S will be nearly 0.10 to 0.72.

3.4.3 BASIC FUNCTIONAL BLOCKS OF THE RELAY:

This is shown in figure(3.3) .The essential features of the blocks are described below

a. A/D/CONVERTER :

This converts an analog input signal into 12 bit- binary number .The conversion starts when control signal comes form the digital controller blocks .At a given instant of time ,one

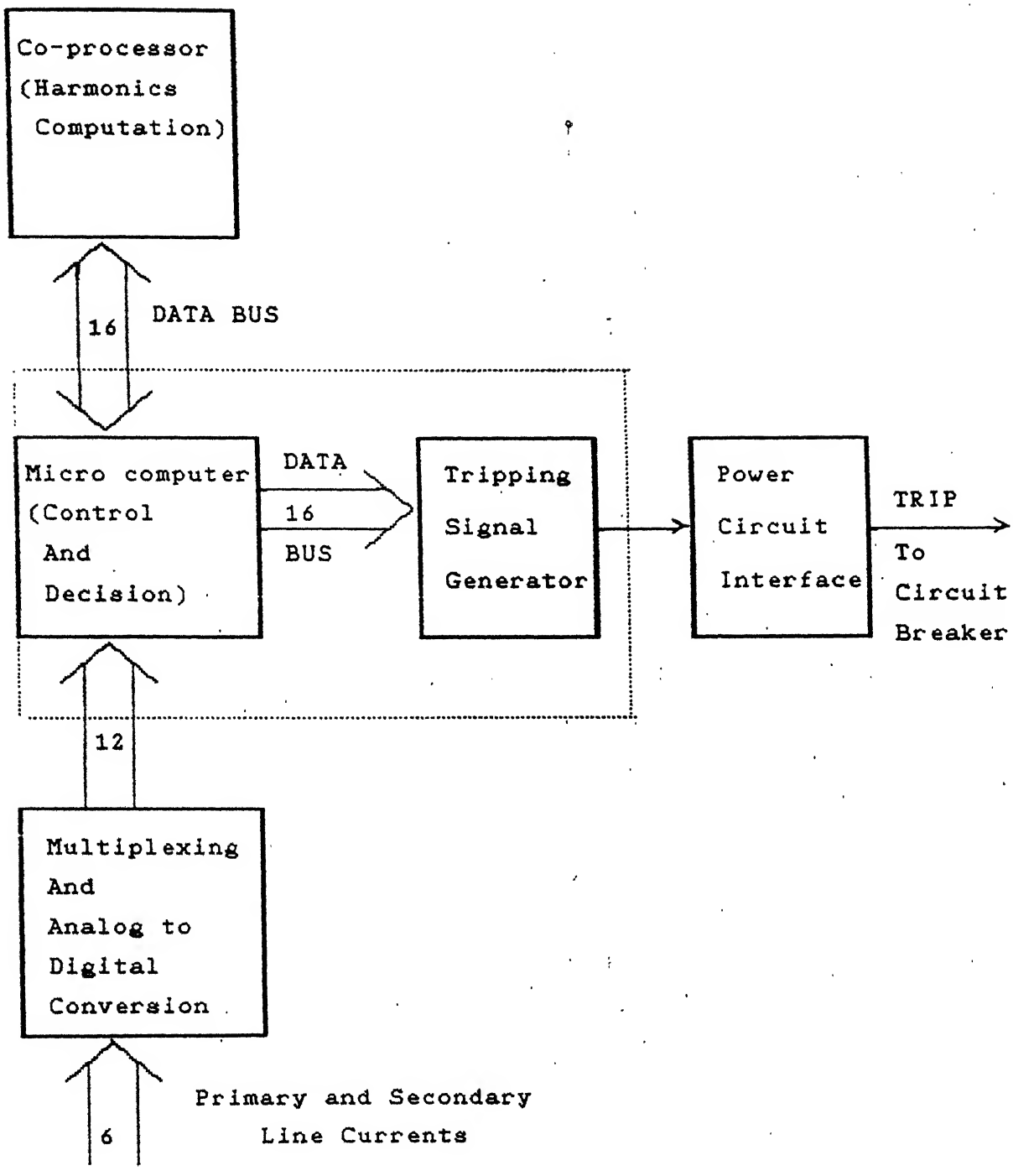


FIG.(3.3) BASIC FUNCTIONAL BLOCKS OF PROPOSED RELAY

of the 6 (in present scheme 2) is selected using 6 channel multiplexer .

b. μP BASED DIGITAL CONTROLLER:

This is implemented in a 16-bit, Intel's 8086 Micro processor .It communicates with other blocks through appropriate control signals.

c. TRIPPING SIGNAL GENERATOR :

This function is performed by microprocessor itself.After performing filtering operation and comparing various harmonic components ,it sends out tripping command (if it so decides) through I/O port to controller block .

d. POWER CIRCUIT INTERFACE :

This consists of current driver stage .It is used to reduce loading on the I/O chip.

3.4.4 DESCRIPTION OF PROPOSED RELAYING SCHEMES:

The detailed block diagram of the relaying scheme is shown in Fig.(3.).

As discussed earlier ,the current samples are used to take the tripping decision .For sampling ,the current is stepped down by CTs .The current is now passed into air core transformer known as transactor to convert current into voltage signals .One of these 6 signals is passed to the A/D converter ,at any instant .The ADC sends a 12 bit digital output to I/O interface consisting of ports PPI 8255A-1.This

is accomplished by ANDing an End Of Conversion (EOC) signal to the microprocessor via interrupt controller PIC 8259.This signal interrupts the microprocessor which invokes an interrupt service routine (ISR) to fill the current data from A/DC into one of its buffers.After filtering data from one channel,a channel select signal to next channel of the MUX and a convert start pulse is issued to ADC by microprocessor through ISR.A second buffer stores the second channel data,and so on for all channels .The channel inputs are taken from two windings of the transformer .Initially 16 samples are stored and afterwards each oldest sample is replaced by the new sample.Thus the main program always finds the buffer full.The main program performs filter and decisive operations using these buffer data and outputs its decision of tripping or no tripping.

A Timer (8253) is programmed for outputting Convert Start pulse to A/DC at the required sampling intervals (20/16).The whole process,starting from filling in the buffer with latest data,is closed looped.

The design of the relay involves two aspects- Hardware and Software development.These are briefly discussed in the following para.

3.4.5 HARDWARE DEVELOPMENT :

The detailed working of various blocks of Fig.(3.4) is described below.

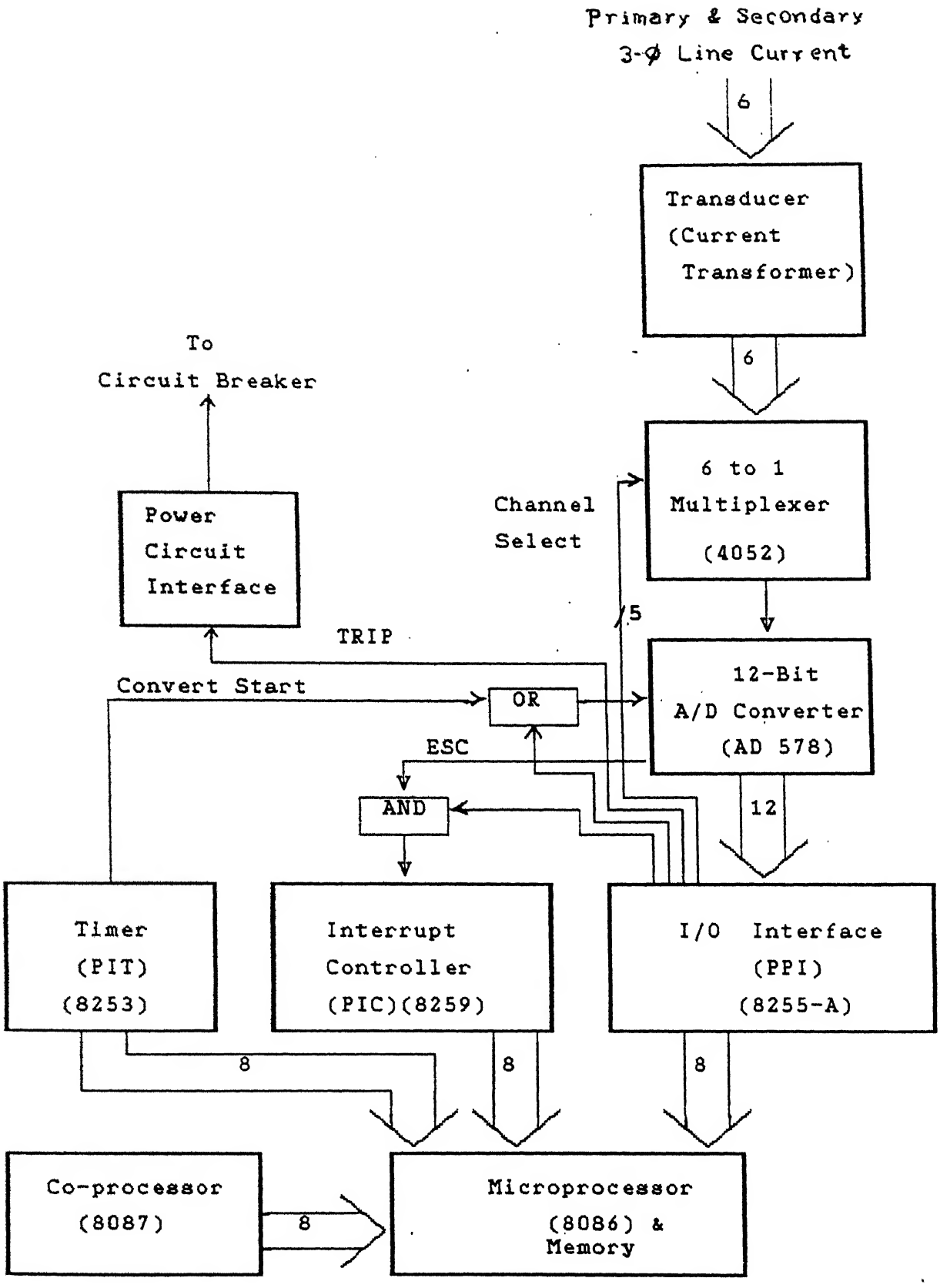


FIG.(3.) DETAILED BLOCK DIAGRAM OF THE RELAY

a. MEASUREMENT AND DETECTION:

It consists of three sections-Transducer,Multiplexer and 12 bit A/D Converter as shown in Fig(3.5).

b. TRANSDUCER :

The circuit diagram of transducer is shown in Fig. (3.).The primary and secondary line currents are stepped down using Current Transformer.These current signals are sensed by converting into voltage signals using Sensing Registers or transactors.These signals,proportional to currents flowing through them,are fed to MUXes after passing them through isolation transformers.

c. MULTIPLEXER :

The six voltage signals are the input to two MUXes (4052).Output of these goes again to a third MUX outputting one channel at a time. The MUX channel are controlled using channel select control word from PPI-8255 port C (lower). Table (3.) shows the combination of channel select bit used for selecting the channels.

d. A/D CONVERTER :

The analog signal from the channel , selected by MUX reaches ADC (AD 578) which converts the analog signal into an equivalent 12-Bit digital signal. The AD-578 has been connected in bipolar mode($\pm$5V) to read both positive and negative values of the analog signals and gives minimum conversion time of approx.3μs. A convert start pulse generated

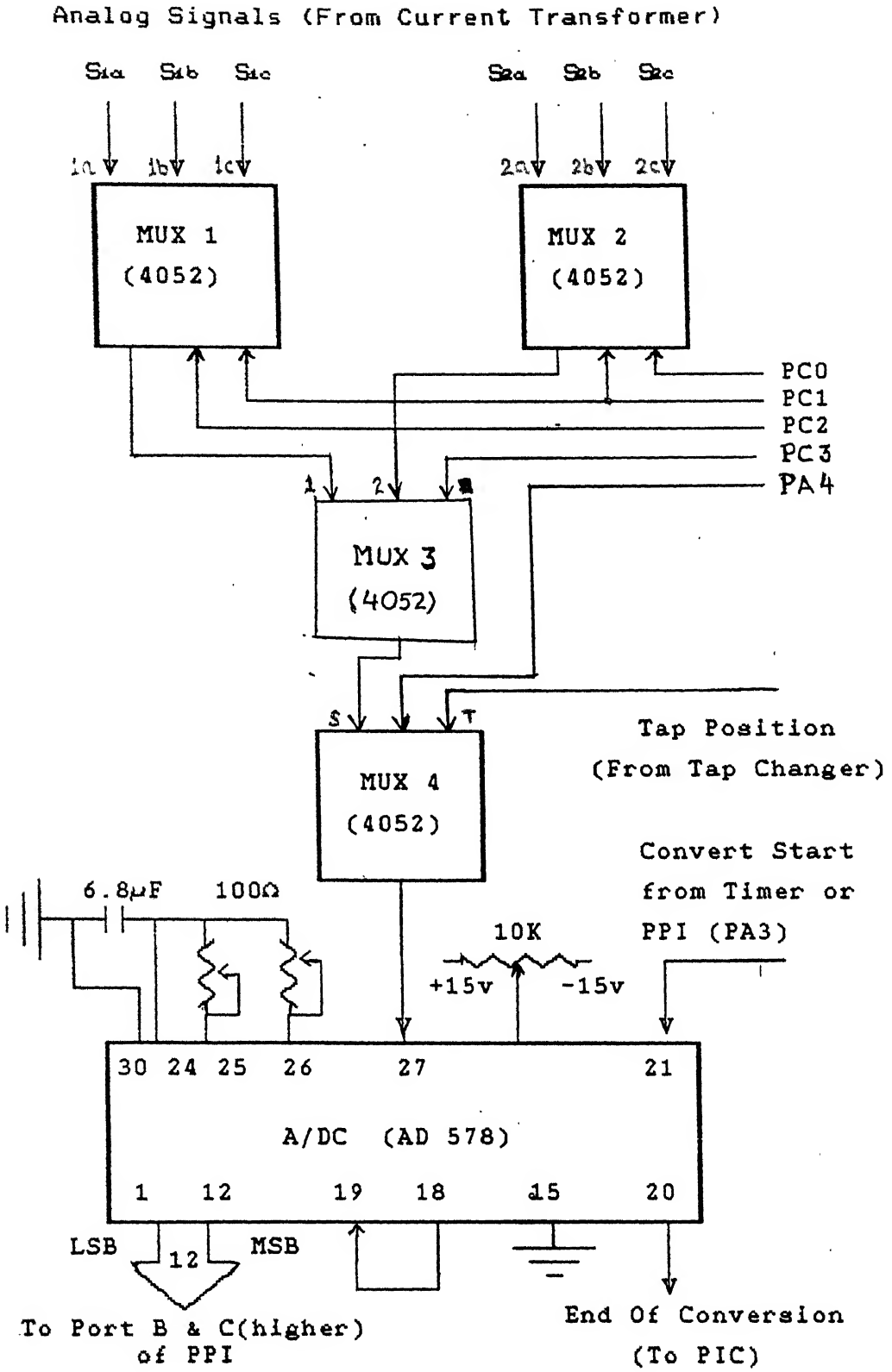


FIG (3.) 6 TO 1 MULTIPLEXING AND A/D CONVERSION

by timer (8253) starts the conversion at its falling edge.The 12-bit output isread by software through ports B and C(lower) of PPI-8255 and is stored in memory buffer for further processing.

e. I/O INTERFACE AND MICROCOMPUTER

The I/O interface ,a link between external circuit and microcomputer, comprises programmable interrupt controller (PIC 8259) , a programmable peripheral interface (PPI 8255) and a programmable interval timer (PIT 8253). A PPI consists of three programmable ports A, B, C as inputs and outputs. PIC 8259 , PPI and PIT are connected to microprocessor by an 8-bit bidirectional data bus. They are also connected to the appropriate control lines, Fig. (3.6) . After interrupt request (intr) is received by μP and ISR is executed to fill the buffers as explained earlier.

Pt. B and C (lower) programmed as input ports, are used for receiving for 12-bit digital word from the output of ADC. Pt. C's bits are used for outputting control signals in the present work. The configuration is given in table 3. .

The timer is programmed to output the convert start pulse to ADC at an interval of 20/16 ms. The BCD count used for this purpose is 2048.

16-bit Intel-8086, Vinytics kit is used as microcomputer. This is connected to PC-XT through a serial interface using RS-232 connector. The kit and PC are interfaced by a software package named as PC-KIT , developed in the department of Electrical Engg. at IIT Kanpur. The

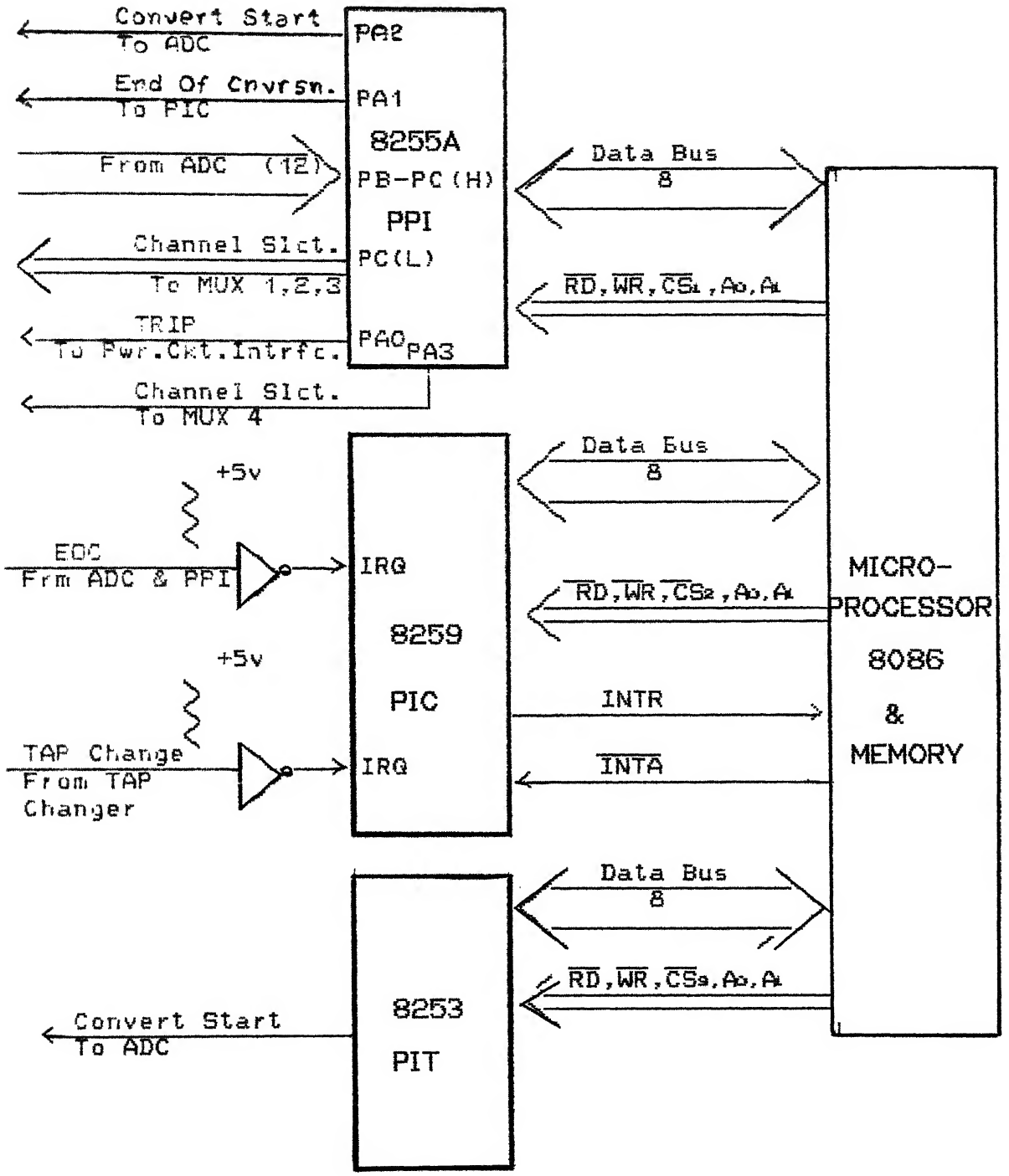


FIG.(3.) I/O INTERFACE AND MICROCOPROCESSOR

software enables easy development of assembly language prog on the PC using Microsoft Assembler and executing the code after downloading it into the kit,i.e.,it provides an interactive environment for the kit through PC-XT.

f. POWER CIRCUIT INTERFACE

It is an intermediary stage between the control circuit and power circuit as shown in Fig.( ),the output tripping signal is passed through a transistor Darligton pair to provide current boost ,thus reducing loading on I/O chip.

3.4.6 SOFTWARE:

This section explains briefly the S/W developed to realize digital relaying scheme.There are two sub-sections:

-Main Program

-ISR Program

a. MAIN PROGRAM :

Flow Chart of main program is shown in FIG.(3.8).This program initializes all I/O Ports,counter,interrupt controller. A flag set by ISR then read . The processing starts , the decision is taken and then μP executes wait loop till interrupt occurs.

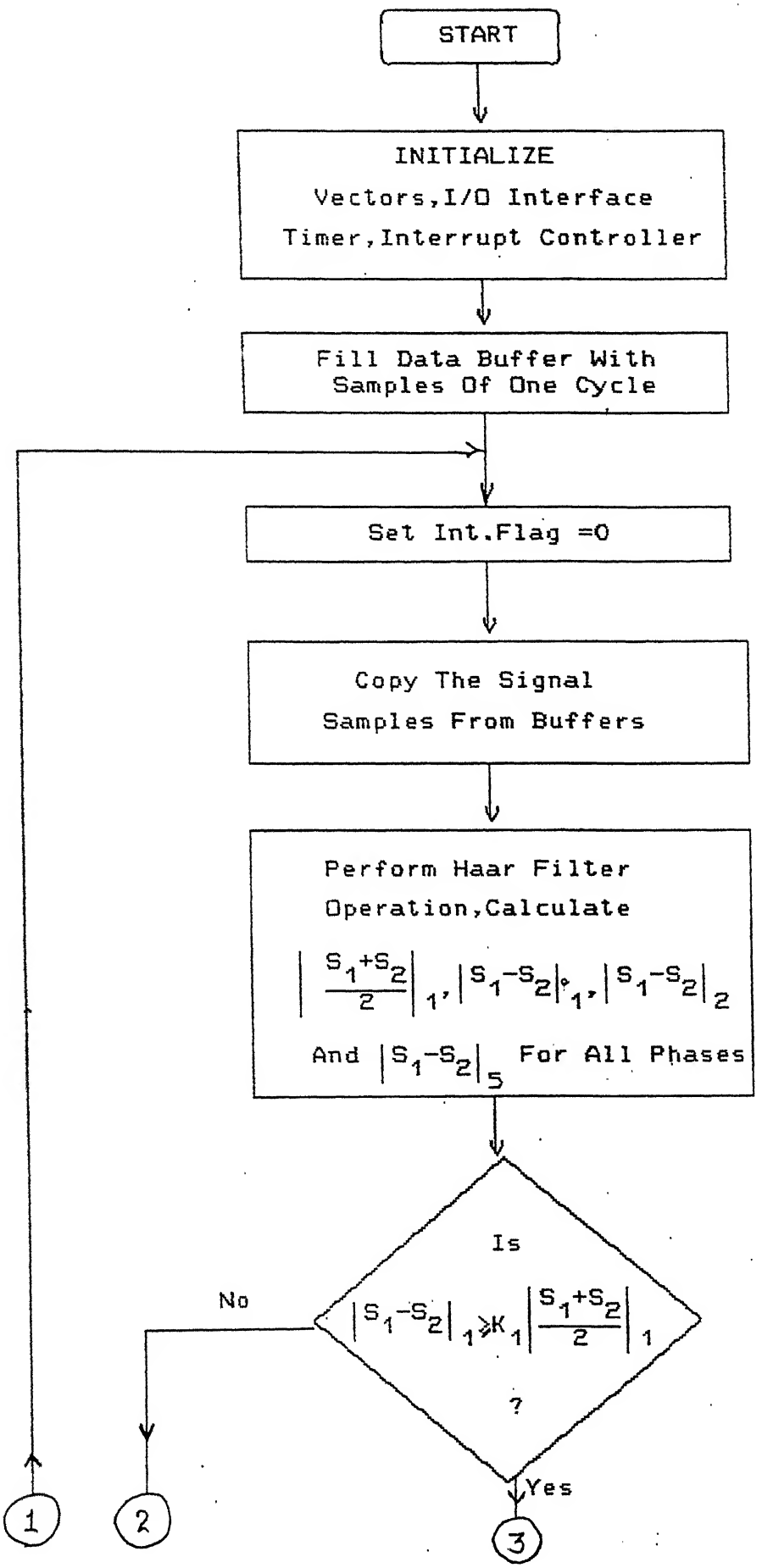
b. ISR :

This is shown in Fig. (3.9). This Program starts getting executed after μP receives an interrupt from from ADC through PIC tasking the μP to input the latest data of the currently

active channel . After filling in the data in a buffer another channel is enabled and similarly its data is also started. Finally the channel is set to the original value and ISR returns control to main program.

3.5 CONCLUSION :

The proposed relaying scheme using 8086 μP has been designed, fabricated and tested in the lab. The relaying scheme is reliable efficient and fast in operation. It gives trip command within 10ms.


START
INITIALIZE
Vectors,I/O Interface
Timer,Interrupt Controller
Fill Data Buffer With
Samples Of One Cycle
Set Int.Flag =0
Copy The Signal
Samples From Buffers
Perform Haar Filter
Operation,Calculate
$\left|\frac{S_1+S_2}{2}\right|_1$, $|S_1-S_2|_1$, $|S_1-S_2|_2$
And $|S_1-S_2|_5$ For All Phases
Is
$|S_1-S_2|_1 \geq K_1 \left|\frac{S_1+S_2}{2}\right|_1$
?
No
Yes
1
2
3

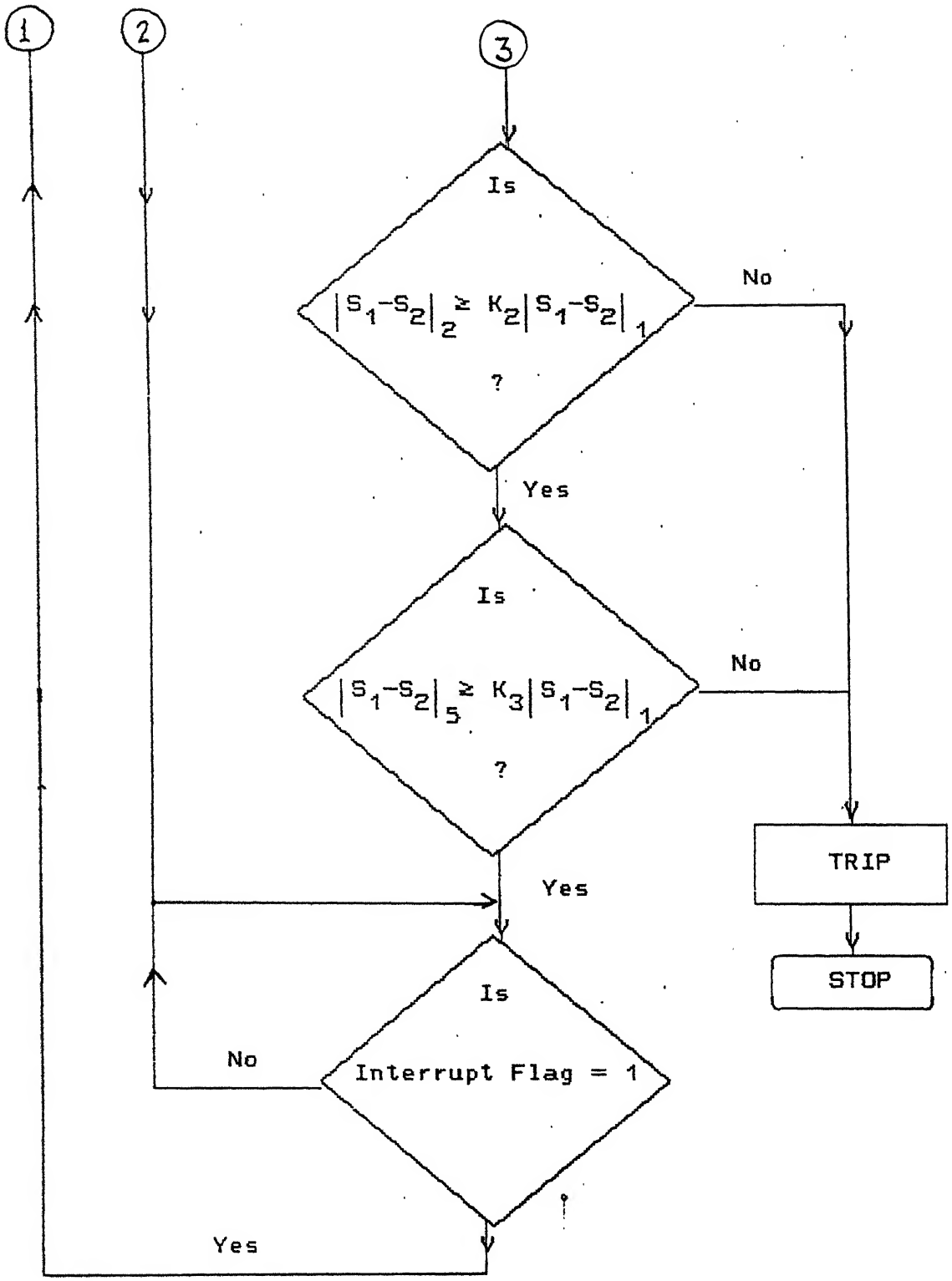


FIG.(3. 8) MAIN PROGRAM FLOW CHART

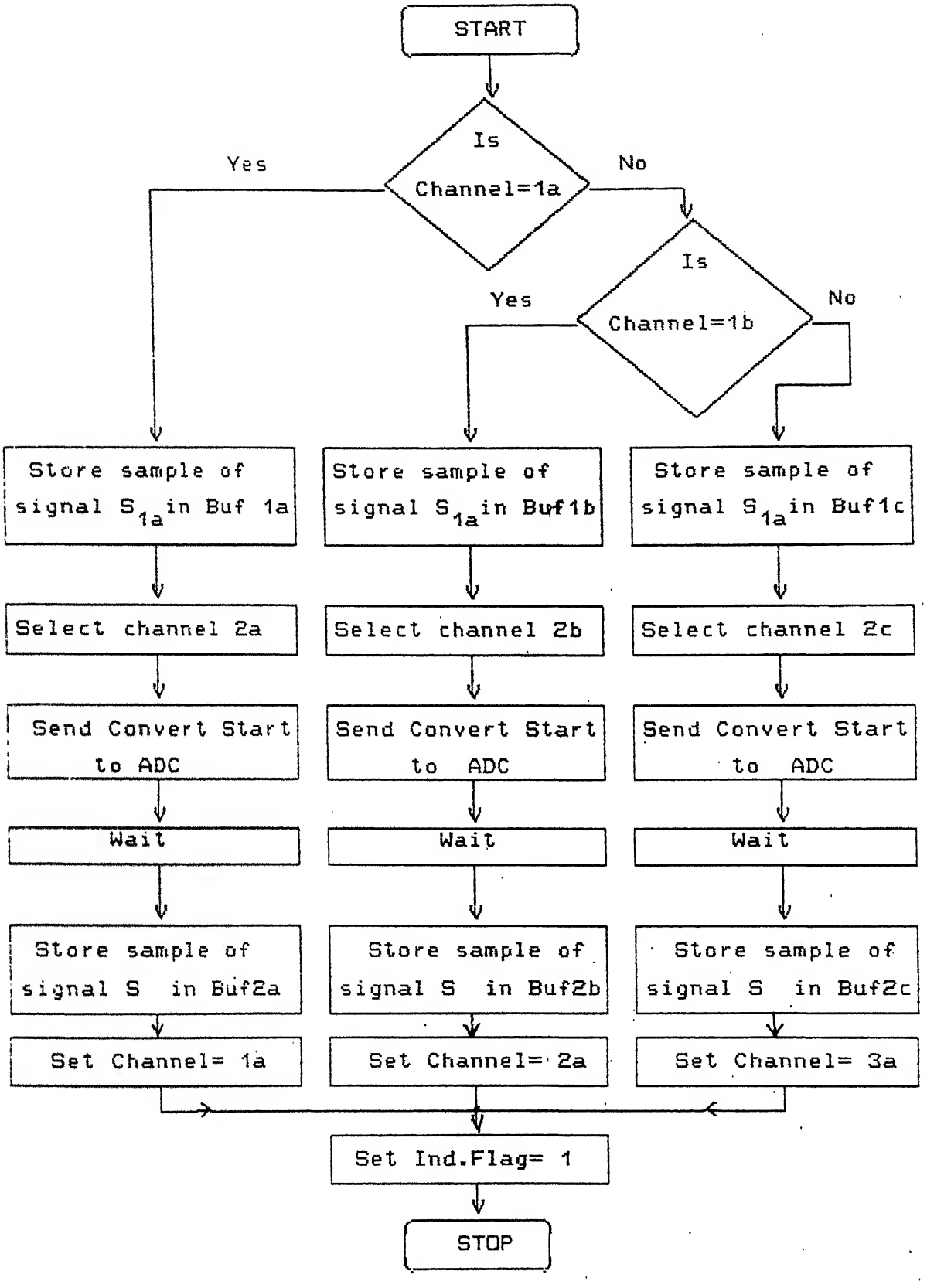


FIG.(3.9) ISR FOR FILLING BUFFERS (3-ϕ XMER)

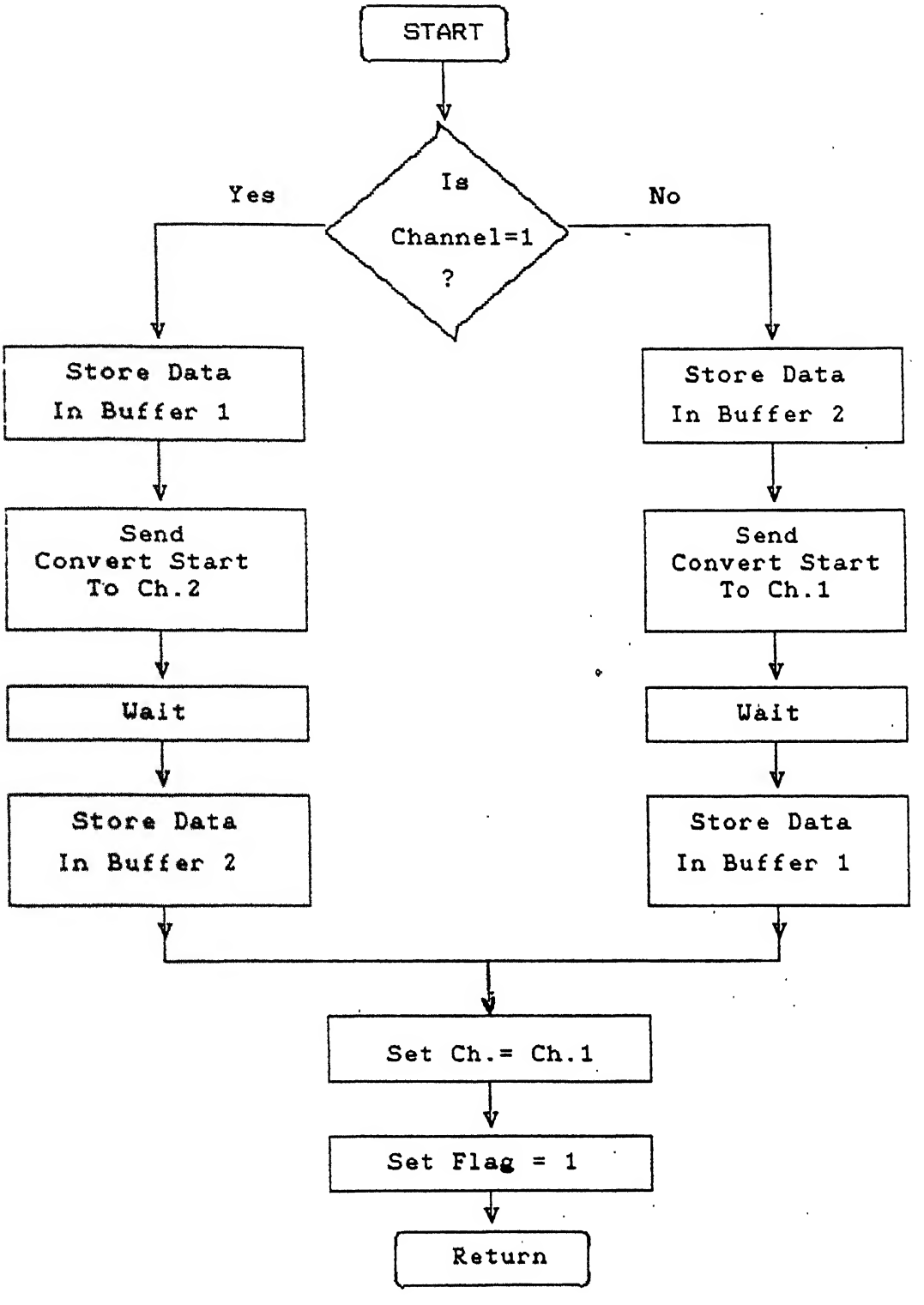


FIG.(3.) ISR FOR FILLING BUFFERS (1-Φ XMER)

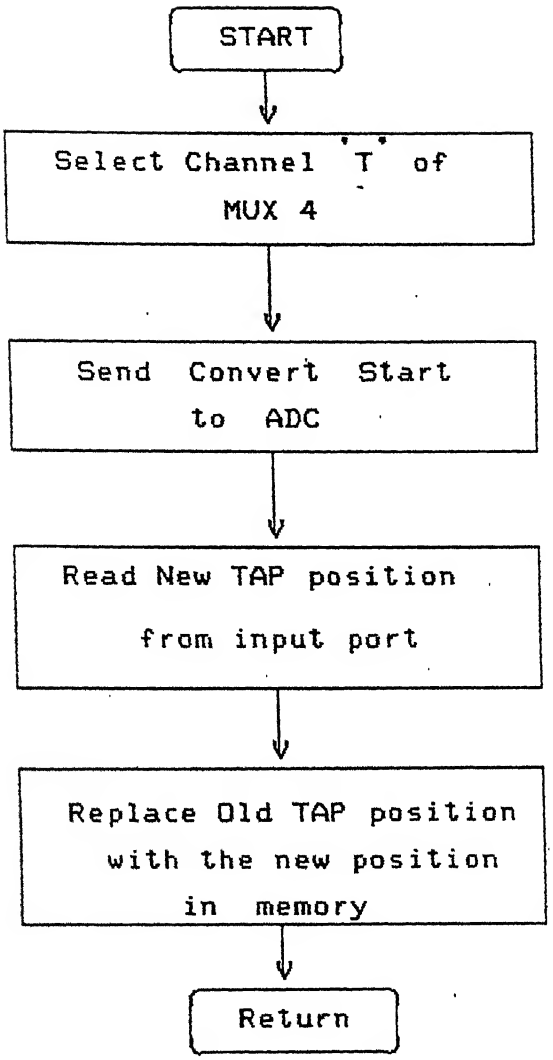


Fig.(3.10) ISR FOR SENSING TAP POSITION

CHAPTER 4

CONCLUSION

The present work has been devoted to the design fabrication and testing of a microprocessor based digital percentage differential relay for transformer protection, using harmonic restraint to avoid tripping due to magnetization and overvoltage inrush currents.The hardware realization uses a 16-bit microcomputer consisting of a microprocessor (Intel 8086) and a floating point co-processor (Intel 8087).Digital signal processing techniques have been used,giving more flexibility,reliability and high speed of operation.

The main objective of hardware optimization and fast speed have been achieved to a large extent. Though,the implementation is for single phase transformer,it can be done for three phase transformer (as shown in the detailed circuit diagram earlier) by incorporating two more MUXes and slightly different system configuration. The software will include storage of data and filtering operation for each of the three phases.

Unique features like provision for taking tap changing into account and variable bias factor for greater sensitivity have been incorporated in this design. A 16 sample Haar Transformation is used to achieve the protection against overvoltage inrush current which could not be possible by using 8 samples.

The relay requires very little power to operate and hence will impose very low burden on CTs used for monitoring line currents.Small changes in components value are hardly expected to cause any change in the relay performance.Hardware complexity is minimal.

The tests and simulations performed indicate that the relay can be expected to do well up to the requirements in the actual field operations.

One limitation of the relay is its high sensitivity to frequency variations.Frequency response of Haar filters shows that the attenuation of undesirable harmonics decreases sharply as the operating frequency changes from 50 Hz.For this reason the relay may be expected not to perform satisfactorily under significant frequency variations.

The above mentioned limitations can be overcome by using a different transformation technique instead of Haar in the filter portion of the relay,viz. Walsh Transformation.

The self checking feature is also included in the relay.

With a little more addition in hardware,the relay can also take care of the faulty or no operation of tripping devices,auxiliary power supplies,current transformers,etc, thus checking all elements of the protection scheme.

Finally,the work can be extended to provide protection of more than one transformers in sub-stations or power plants,using a modified relay hardware and software.

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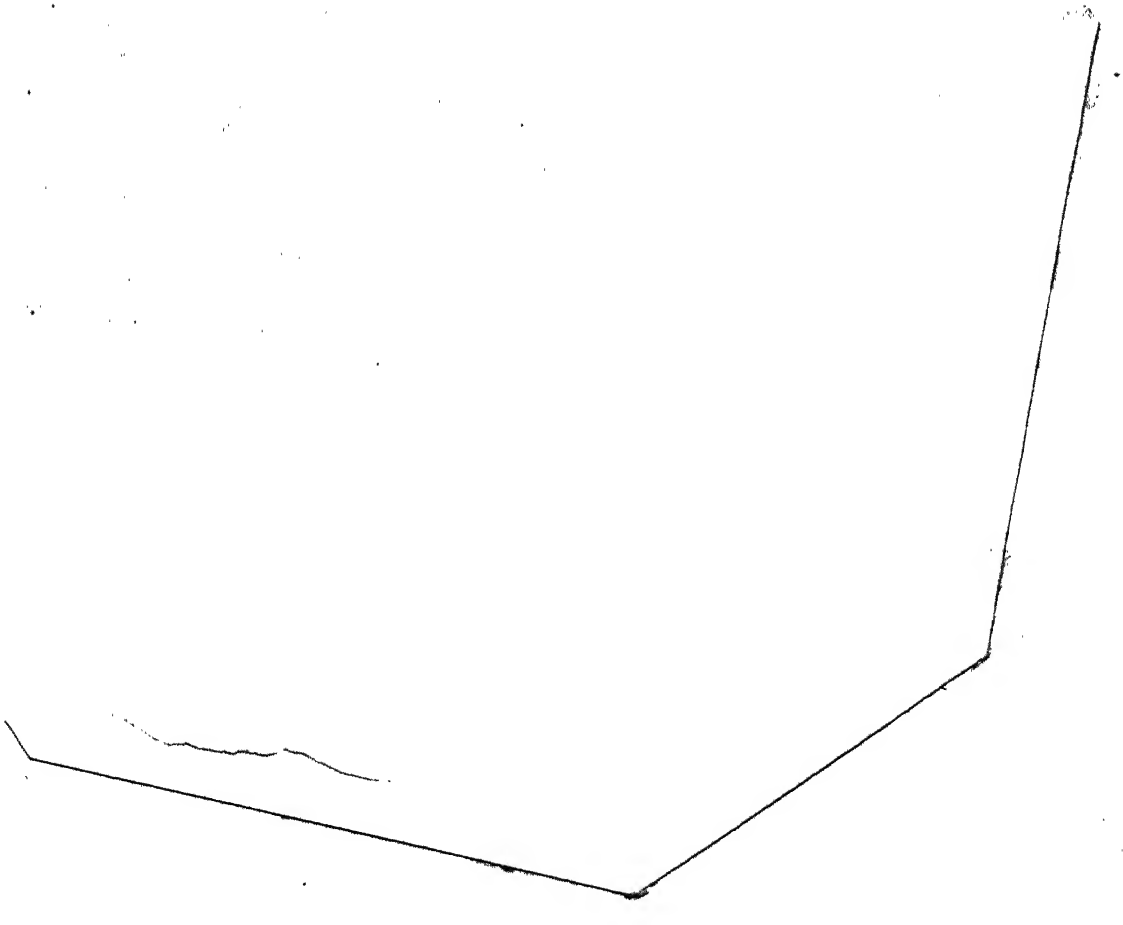
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